REMARKS

Applicants have learned the previous arguments with respect to claims 7-15 which have been considered but are deemed moot in view of the new grounds of rejection.

Claims 7-15 are pending and have been rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. (USPN 6,445,011; "Hirano" hereinafter) in view of Tominaga (USPAP 2002/0008325; "Tominaga" hereinafter) and further in view of Okazaki et al. (USPN 5,298,768; "Okazaki" hereinafter).

Applicants have amended claims 7, 12, 14, and 15 according to FIG. 3 and paragraph [0023] reciting that "...The semiconductor sub-mount 200 comprises an N-doped silicon substrate (not labeled), a P-doped region 208 and an insulating layer 206..." in the specification of the present invention and have combined claim 13 into claim 7 to more clearly define the present invention and respectfully traverses the rejections for the reasons given below:

Referring to FIG. 11B and the description on column 11, lines 21-27 of Hirano's specification, the positive electrode 422, as purportedly reading on the patterned conductive-reflective film 210 of the instant case, is formed on the insulation film 424 and electrically connected to the n-layer (semiconductor substrate) 443 via the windows formed in the insulation film 424. Hence, the positive electrode 422 taught by Hirano **directly covers the insulation film 424 but indirectly caps the semiconductor substrate 443**. Nevertheless, referring to FIG. 3 and amended claim 7 of the present invention, the first patterned conductive-reflective film 210 ***directly covers the first sidewall of the cavity and directly covers a part of the first conductive***

type semiconductor substrate, thus yielding clear differences in comparison with the teaching of Hirano in view of Tominaga and Okazaki.

Accordingly, claim 7 should be patentable over Hirano in view of Tominaga and Okazaki, for the cited references of record either alone or in combination fail to teach or suggest that **"the first patterned conductive-reflective film directly covers the first sidewall of the cavity *and directly covers a part of the first conductive type semiconductor sub*strate, and the second patterned conductive-reflective film at least substantially covers the second sidewall of the cavity and is separated from the first conductive type semiconductor substrate by the insulating layer,"** as claimed in Applicant's claim 7, rendering claim 7 unobvious over the prior art references and placing claim 7 and claims 8-12 and 14-15 depending upon the allowable claim 7 all in proper condition for allowance. Reconsideration and withdrawal of the rejection and allowance of the present invention are respectively requested.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 7-15 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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